MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2016/2017

EEN4206 – SEMICONDUCTOR PACKAGING AND TEST

(ALL)

19 OCTOBER 2016
9.00 a.m - 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 3 pages with 4 Questions only.
2. Attempt **ALL (4)** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.

Question 1

(a)(i) Write down the general IC manufacturing process flow. [5 marks]

(ii) In the above process flow, which are 10k and 100k class cleanrooms? [2 marks]

(iii) What distinguishes the differences in packaging between Class 10k versus Class 100k? [2 marks]

(b)(i) What is the input process block for plating process? [2 marks]

(ii) Name two typical plating material types used in semiconductor. [2 marks]

(iii) Why do we need to perform plating for final finishing? [2 marks]

(iv) What is the test condition for Whisker? [3 marks]

(v) What is the potential effect of Whisker in Electronics? Give an example. [2 marks]

(c)(i) What are the categories of packages today based on mounting types? Explain the fundamentals of the mounting types. [3 marks]

(ii) For the categories of packages in part (i), what are the typical application categories of these packages address? [2 marks]

Question 2

(a) Specify key machine parameters that give significant impact on bonding formation and enumerate capillary dimensions that affect the formation in wire bonding process. [3 + 7 marks]

(b) Briefly describe the process steps or process sequences for Solder Paste Die Attach Process and each function of the process steps. [5 marks]

(c) Name the key compositions of Epoxy Mold Compound (EMC). [5 marks]

(d) Provide a description of the equipment module in molding system below:
(i) Leadframe preheater
(ii) Pallet supply unit
(iii) Cleaning unit
(iv) Mold press
(v) Degating and transport unit [5 marks]

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Question 3

(a) Describe the role of product engineering. [3 marks]

(b) What are the six major processes at wafer fabrication? [6 marks]

(c) Where is the Process Control Monitoring (PCM) structure located in the wafer? Use drawing to indicate it. [4 marks]

(d) What is the purpose of the PCM Test? What are the four most common tests at PCM test? [2 + 4 marks]

(e) Explain the function of the labels (i), (ii) and (iii) in the wafer probe system functional test setup in Fig. Q3. [6 marks]

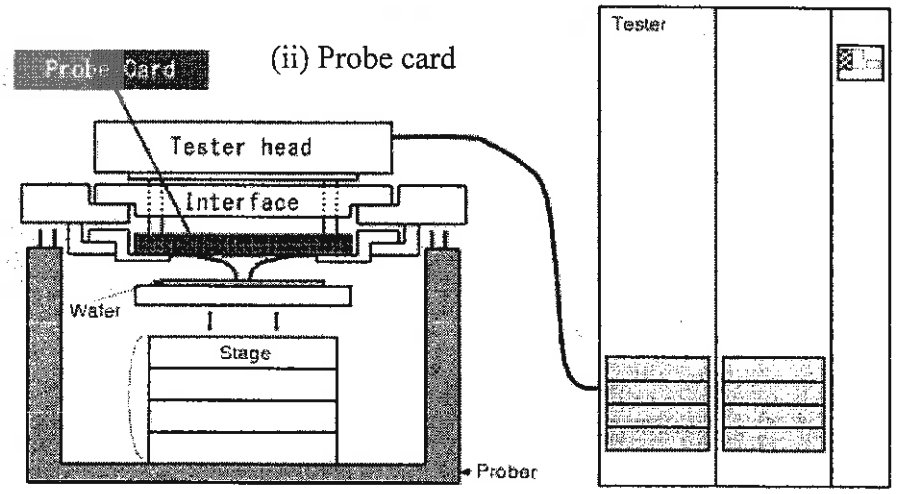

Figure Q3

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Question 4

(a)(i) What are the imaging techniques available in failure analysis? [2 marks]

(ii) Write down the working principle of each technique listed in part (i). [2 marks]

(b) What are the sample preparation methods available in failure analysis? [3 marks]

(c)(i) What is thermal hot spot in semiconductor? [2 marks]

(ii) What are the techniques used to investigate thermal hot spot? [2 marks]

(d)(i) Define acceleration factor. [2 marks]

(ii) Explain the meaning of acceleration factor and "same result" in acceleration factor. [3 marks]

(iii) What is the key assumption in accelerated testing in terms of failure mode and/or mechanism? [2 marks]

(e)(i) What kind of extreme environmental conditions for semiconductor device to be exposed once it is put in real world applications? [3 marks]

(ii) What are the internal stressors experienced by semiconductor device when subjected to external stressors like voltage and current in the table below? [4 marks]

External stressors	**Internal stressors on device**
Voltage	•
Voltage & Current	•
Current	•
	•

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